Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 44-79, as follows:

Listing of Claims:

1-43. (Cancelled)

44. (New) A method of generating first and second internal memory addresses from an external memory address for accessing memory locations in respective memory arrays corresponding to the external memory address, the method comprising:

generating a predecode address having a predecode sequence of binary digits, the predecode sequence based on a portion of the external memory address;

in response to the external memory address having an even value, providing the predecode address in the predecode sequence as the first and second internal memory addresses; and

in response to the external memory address having an odd value, providing the predecode address in the predecode sequence as the first internal memory address, changing the predecode address into a modified sequence, and providing the modified predecode address as the second internal memory address.

45. (New) The method of claim 44 wherein shifting the predecode address into a modified sequence comprises shifting the predecode address to result in the first and second internal memory addresses having sequential values.

46. (New) The method of claim 44, further comprising receiving a burst length command having a burst length value, and wherein shifting the predecode address into the modified sequence is based on the external memory address having an odd value and the burst length value.

47. (New) The method of claim 46, further comprising generating first and second pairs of internal memory addresses in response to a first burst length value and generating first, second, third and fourth pairs of internal memory addresses in response to a second burst length value.

48. (New) The method of claim 44 wherein generating a predecode address comprises generating an address value having all but one of the bits at a first value.

49. (New) The method of claim 48 wherein shifting the predecode address into a modified sequence comprises shifting the bit of the predecode address not having the first value to a different bit location.

50. (New) The method of claim 44 wherein N bits of the external memory address are used to generate the predecode address and the predecode address is 2**N bits in length.

51. (New) The method of claim 50 wherein N is equal to three.

52. (New) In a memory device, a method of generating a pair of internal burst addresses for a burst operation from an external memory address, the method comprising:

generating a plurality of predecode signals having logic levels based on the external memory address;

applying the predecode signals as the first of the pair of internal burst addresses; and

based on the value of the external memory address, applying the predecode signals as the second of the pair of internal burst addresses in response to the external memory address having a first value, and in response to the external memory address having a second value, rerouting the predecode signals into a reordered arrangement to be applied as the second of the pair of internal burst addresses.

53. (New) The method of claim 52 wherein the first value is an even value and the second value is an odd value.

54. (New) The method of claim 52 wherein rerouting the predecode signals comprises shifting the order of the bits of the predecode signals before applying the shifted bits as the second of the pair of internal burst addresses.

55. (New) The method of claim 52, further comprising receiving a burst length command having a burst length value, and wherein rerouting the predecode signals is based on the external memory address having the second value and the burst length value.

56. (New) The method of claim 55, further comprising generating first and second pairs of internal addresses in response to a first burst length value and generating first, second, third and fourth pairs of internal addresses in response to a second burst length value.

57. (New) The method of claim 52 wherein generating the plurality of predecode signals comprises generating plurality of predecode signals based on N bits of the external address.

58. (New) The method of claim 57 wherein the predecode signal is 2**N bits in length.

59. (New) A method for generating internal memory addresses in response to receiving an external memory address, the method comprising:

predecoding the external memory address;

providing the predecoded external memory address as a first internal memory address; and

providing the predecoded external memory address as a second internal memory address in response to an even valued external memory address; and

reordering the sequence of bits of the predecoded external memory address and providing the reordered predecoded external memory address as the second internal memory address in response to an odd valued external memory address.

60. (New) The method of claim 59 wherein reordering the sequence of bits of the predecoded external memory address comprises shifting the order of the bits of the predecoded external memory address before applying the shifted bits as the second internal memory address.

61. (New) The method of claim 59, further comprising receiving a burst length command having a burst length value, and wherein reordering the sequence of bits is in response to an odd valued external memory address and based on the burst length value.

62. (New) The method of claim 61, further comprising generating first and second pairs of internal memory addresses in response to a first burst length value and generating first, second, third and fourth pairs of internal memory addresses in response to a second burst length value.

63. (New) The method of claim 59 wherein predecoding the external memory address comprises predecoding the external memory address based on N bits of the external memory address.

64. (New) The method of claim 63 wherein the predecoded external memory address is 2**N bits in length.

65. (New) A method for generating internal memory addresses in response to receiving an external memory address, the method comprising:

predecoding N bits of the external memory address to generate a 2**N bit predecode address having one active bit;

applying the 2**N bit predecode address as a first internal memory address for accessing a first memory array; and

in response to the least significant bit (LSB) of the external memory address is equal to zero, applying the 2**N bit predecode address as a second internal memory address for accessing a second memory array, and in response to the LSB of the external memory address is equal to one, reordering the sequence of bits of the 2**N bit predecode address to a modified sequence of 2**N bits and applying the modified 2**N bits as the second internal memory address.

66. (New) The method of claim 65 wherein N is equal to three.

67. (New) The method of claim 65 wherein predecoding N-bits of the external memory address comprises generating a predecoded memory address having all but one of the bits at a first value.

68. (New) The method of claim 67 wherein reordering the sequence of bits of the predecode address comprises shifting the bit of the predecoded memory address not having the first value to a different bit location.

69. (New) The method of claim 65 wherein reordering the sequence of bits of the predecode address comprises shifting the predecode address to result in the first and second internal memory addresses having sequential values.

70. (New) The method of claim 65, further comprising receiving a burst length command having a burst length value, and wherein reordering the sequence of bits of the predecode address is based on the burst length value.

71. (New) The method of claim 70, further comprising generating first and second pairs of internal memory addresses in response to a first burst length value and generating

first, second, third and fourth pairs of internal memory addresses in response to a second burst length value.

72. (New) A method for generating internal memory addresses for a burst memory operation from an external memory address, the method comprising:

predecoding the external memory address into a predecoded address;

providing the predecoded address as first and second internal memory addresses in response to the external memory address being an even value; and

in response to the external memory address being an odd value, providing the predecoded address as the first internal memory address, reordering the bit sequence of the predecoded address and providing the reordered predecoded address as the second internal memory address, the predecoded address and the reordered predecoded address sequential in value.

73. (New) The method of claim 72 wherein reordering the bit sequence of the predecoded address comprises shifting the predecoded address to result in the first and second internal memory addresses having sequential values.

74. (New) The method of claim 72, further comprising receiving a burst length command having a burst length value, and wherein reordering the bit sequence is based on the burst length value.

75. (New) The method of claim 74, further comprising generating first and second pairs of internal memory addresses in response to a first burst length value and generating first, second, third and fourth pairs of internal memory addresses in response to a second burst length value.

76. (New) The method of claim 72 wherein predecoding the external memory address comprises generating an address value having all but one of the bits at a first value.

77. (New) The method of claim 76 wherein reordering the bit sequence of the predecoded address comprises shifting the bit of the predecoded address not having the first value to a different bit location.

78. (New) The method of claim 72 wherein N bits of the external memory address are used for predecoding the external memory address and the predecoded address is 2**N bits in length.

79. (New) The method of claim 78 wherein N is equal to three.